EMC Design Tips

Bruce Archambeault, Associate Editor

Welcome to Design Tips! Recently I was talking to a colleague who mentioned that we (as a Society) seem to always focus on very high speed boards, with many layers, etc. But we seldom discuss boards that are much simpler in construction, such as single layer boards. So in this issue, I will discuss printed circuit boards that have no solid planes. The concepts are the same as with boards with solid planes, but the implementation is different!

Please send me your most useful design tip for consideration in this section. Ideas should not be limited by anything other than your imagination! Please send these submissions to bruce.arch@ieee.org. I'll look forward to receiving many "Design Tips!" Please also let me know if you have any comments or suggestions for this section, or comments on the Design Tips articles.

You will also find "Design Tid-Bits" at the end of the Design Tips Article. These Tid-Bits are intended to be a very short description of EMC design best practices and cover a wide range of EMC design issues. Please send me your contributions to bruce.arch@ieee.org.

Boards Without Solid Planes

One and two-layer boards present a definite challenge for EMC design. While 'generic' EMC design rules claim this stack-up is not recommended, it is often selected for considerations other than EMC, such as low cost, etc. With this stack-up, there are normally no solid planes and all signals, power and returns (sometimes called 'ground'[1]) are routed as traces. While the signal speeds on these boards are normally less than might be expected on the multilayer boards with solid planes, they can still cause EMC problems. The main EMC concern in this design strategy is to keep the loop area for the signal current as small as possible and not allow large loop areas for current as illustrated in Figure 1. Remember, the current must always return to its source, and the return path creates part of this total loop.

The loop shown in Figure 1 is not a simple rectangle, and so there is no simple formula to calculate the strength of the radiated fields; however, if we examine the formula for an electrically small simple loop we can see the direct relationship of the radiated fields and the loop area. Equation 1 [1] gives the electric field strength in the far field for a small loop antenna. The electric field strength increases/decreases in direct proportion to the area (A) of the loop.

$$E_\phi = \frac{120\pi^2 [I] \sin\theta}{r\lambda^2} A$$

where:

A is the area of the loop

I is the current amplitude at the frequency of interest

r is the distance to the observation point

θ is the angle to the observation point

and λ is the wave length of the frequency or interest.

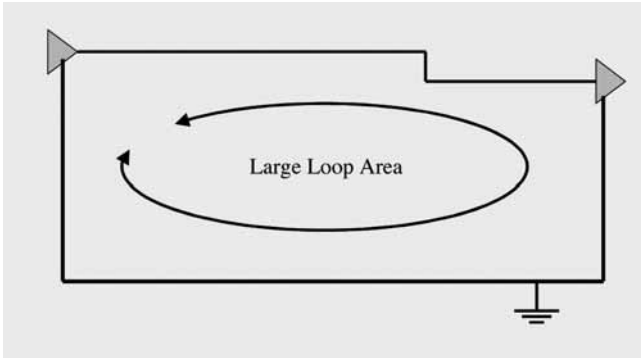

Figure 1. Example of Single Sided PCB Routing with Large Loop Area for Signal Current

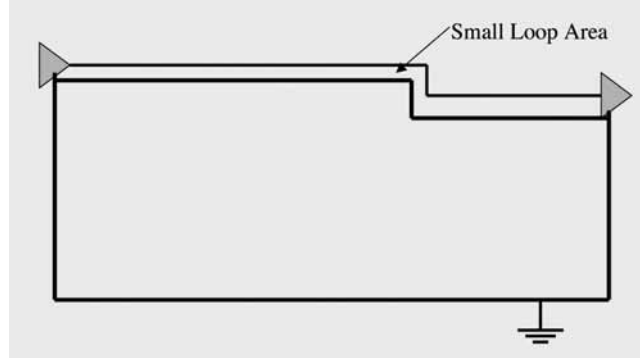

Figure 2. Example of Single Sided PCB Routing with Small Loop Area for Signal Current

There is reciprocity between an antenna that is transmitting or receiving. So this means that for a given field strength of an impressed field (for immunity testing, for example), the amount of current that will be induced in the loop is also directly proportional to the area of the loop. Larger loops will be likely to cause more susceptibility problems than smaller loops. The area of the loop is the key!

To minimize this problem, the signal return trace should be routed along side the signal trace to minimize the loop area. Figure 2 shows an illustration of this design strategy. Note that the GND trace is still present in Figure 2, but no significant return currents will flow in the GND trace at the lower part of the board. Current will always take a path that minimizes its impedance. This means that the current will take the path of least inductance (at frequencies above a few 10's of KHz). Minimizing the loop area also minimizes the inductance, so the return current will flow in the return path nearest to the signal trace. Keeping signal traces short will also minimize the loop area.

The return current path is often overlooked, since it is not specified in the circuit schematic. Only a connection to some magical conductor called 'ground' is shown on schematics. However, the physical routing of the signal and the return current path must be considered to reduce emissions and immunity problems.

[1]From the Summer 2006 EMC Newsletter Design Tip section, we know that "Ground is a place for potatoes and carrots."

[1] Kraus, John D., Antenna, McGraw-Hill, 1988.

Design Tid-Bit

'Current' causes emissions, not 'voltage'! Voltage is convenient to measure, but current does the work. Always think about the entire path (out and back) for current. When using voltage, remember that there must be TWO conductors and one is reference. So it makes no sense to say: "there is noise voltage on 'ground'" without explaining the noise voltage is relative to some other location. — Bruce Archambeault