Design Tips

Bruce Archambeault, Associate Editor

Welcome to Design Tips! In this issue, I will discuss the effect of mounting multiple decoupling capacitors on a printed circuit board and the equivalent inductance of these multiple capacitors.

Inductance is often misunderstood, but it is a very important concept to understand. Many of you know Dr. Albert Ruehli (formerly with IBM Watson Research Center, and now with the Missouri University of Science and Technology), but you may not be aware that he is the author of one of the fundamental papers on inductance! His paper from 1972 is a pivotal work, and while at first glance it may seem too mathematical for practical applications, it is worth the time to read and understand! I encourage you all to read the paper that is republished in this issue of the EMC Newsletter on page 58 and to also look at the mathematics as a way to help you get a better understanding of inductance. In Dr. Ruehli's paper, he uses the concept of partial inductance to calculate the inductance of various shapes. This concept of partial inductance allowed the current density plots in this Design Tip to be created! These current density plots allow us to better understand the true effective inductance, especially when the current density is not constant over the conductor. Partial inductance is an extremely powerful concept that allows us to assemble the overall loop inductance of non-uniform shapes.

Please send me your most useful design tip for consideration in this section. Ideas should not be limited by anything other than your imagination! Please send these submissions to bruce.arch@ieee.org. I'll look forward to receiving many "Design Tips!" Please also let me know if you have any comments or suggestions for this section, or comments on the Design Tips articles.

Multiple Decoupling Capacitors in Printed Circuit Boards

By Bruce Archambeault, Jingook Kim, Sam Connor, and Jun Fan

In the Spring 2009 issue of the *EMC Newsletter*, the Design Tips showed the typical inductance associated with connecting decoupling capacitors to power/ground-reference planes using standard size surface mount capacitors. Inductance values of 2–3 nH were very typical, even for 0402 size packages; depending on how deep the planes were into the PCB.

It seems reasonable to assume that multiple capacitors connected to the same power/ground-reference planes would reduce the effective inductance in a similar manner as multiple parallel resistors. That is, two capacitors in parallel would have an effective inductance of one-half the inductance of only one capacitor. Recent research [1] has shown that this is not a valid assumption, and that the close proximity of two capacitors does not reduce the effective inductance significantly.

Let's take the case of a single capacitor (represented by port #2 in Figure 1) placed at some distance from an IC power pin (represented by port #1 in Figure 1). Then let's add a second capacitor (represented by port #3) and move this capacitor in a circle around port #1, and find the effective inductance seen by port #1. We will replace the actual capacitor with a perfect capacitor (a shorting via between the planes).

There are different ways to calculate this effective inductance and the mutual inductances between the vias. In [1] the full wave cavity resonance formulation is used and the individual loop inductance and the mutual inductances are found[1]. Once the math is completed, the final effective inductance can be found with the equation (1).

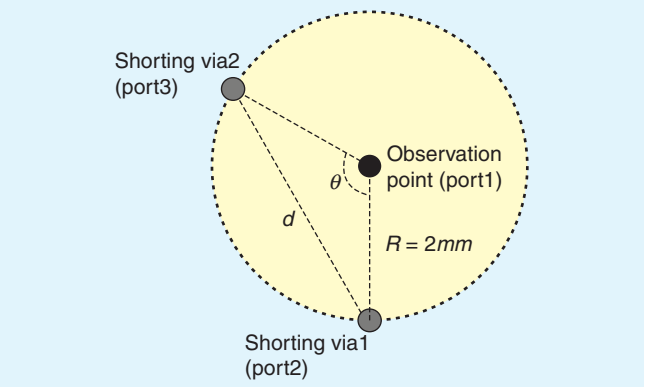

Fig. 1. Shorting via around a circle configuration.

$$L_{eq_circle} = \frac{\mu d}{4\pi} \ln\left(\frac{(R+r)^4}{(2R\sin(\theta/2)+r)r^3}\right) \qquad (1)$$

[1] Readers are referred to the reference to see the straightforward math to calculate the effective inductance.

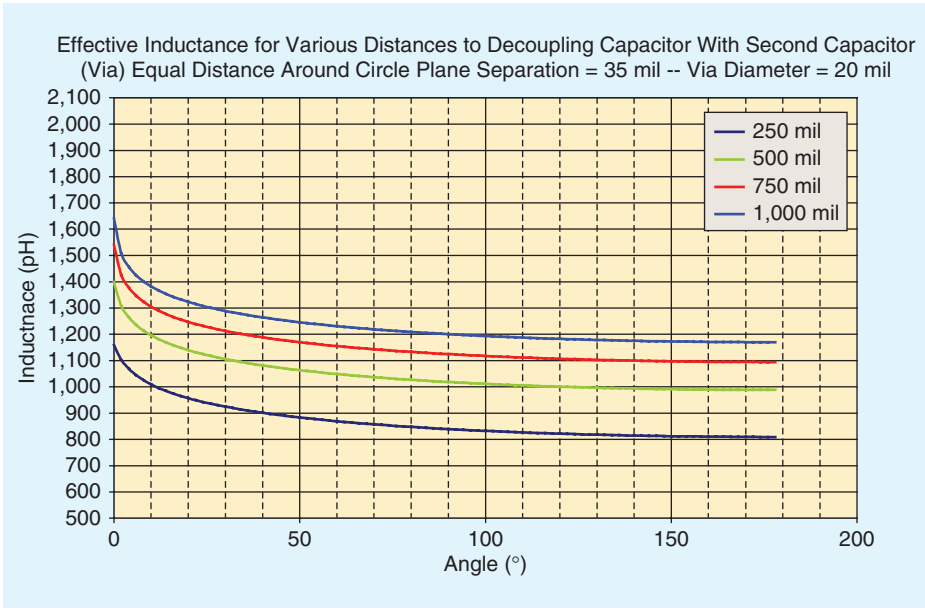

Fig. 2. Effective inductance as second shorting via travels around a circle (plane separation = 35 mils).

loop area that the current travels and the current density. Using the concept of partial inductance[2] [2] [3] we can find the current density in the planes for different positions of the second shorting via. Figure 5 shows the configuration, and Figure 6 shows the current density in the plane. Note that the current density is not equal everywhere, and the current tends to 'bunch' near the ports. As the second shorting via is moved further from the initial shorting via, the current density between the center port and the shorting vias decreases. However, notice that the center port (IC power pin) has the same current density regardless of the position of the second shorting via!

When the current density decreases, the effective inductance will

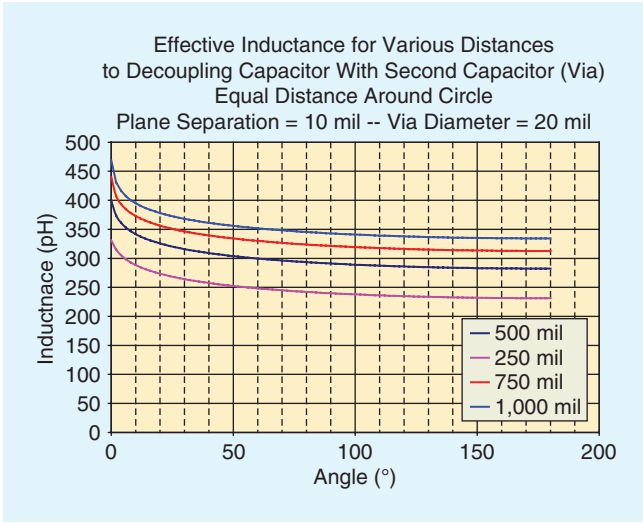

Fig. 3. Effective inductance as second shorting via travels around a circle (plane separation = 10 mils).

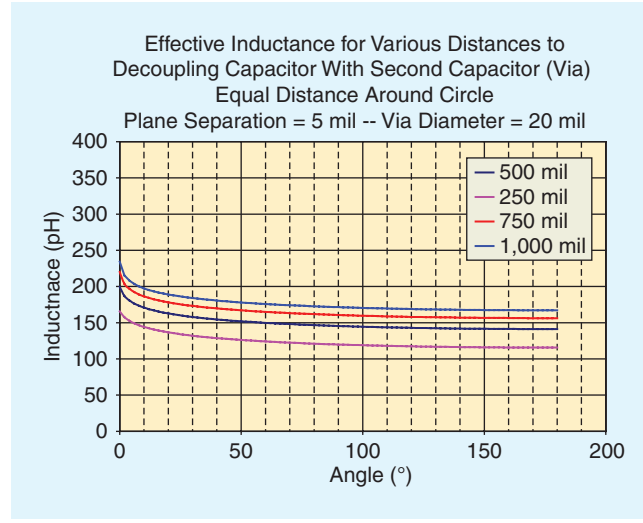

Fig. 4. Effective inductance as second shorting via travels around a circle (plane separation = 5 mils).

Figures 2–4 show the value of the effective inductance for plane separation distances of 35 mils, 10 mils, and 5 mils, respectively. Also the radius of the circle is varied from 250 mils to 1000 mils.

Two things are apparent from Figures 2–4. First, when the angle between ports #2 and #3 is zero, this represents the case of a single shorting via. If the second shorting via is moved further from the single shorting via, the effective inductance decreases, but not immediately. That is, if the second shorting via (perfect capacitor) is close to the first shorting via, the effective inductance is lowered only slightly! As the second shorting via is moved around the circle to the 180 degree position (on the opposite side from the first shorting via) the effective inductance decreases to approximately 70% of the single shorting via case. This holds true for all the power/ground-reference plane distances.

At first, this may seem counter-intuitive, but we must consider that the effective inductance is determined by both the also decrease. However, the effective inductance is comprised of the entire current path. Since the current density near the center port remains high, the effective inductance does not decrease as rapidly as might initially be expected.

We can expand this to the case where two capacitors (shorting vias) are placed side-by-side, and the second shorting via is moved in a straight line away from the first shorting via (shown in Figure 7). Equation (2) modifies the distance in equation (1). Figure 8 shows an example of the effective inductance, showing a similar effect as previously, but the effective inductance does not decrease as much as the circle case since the second shorting via is moving further from the IC power pin.

$$d_1 = \sqrt{R^2 + d_2^2} \qquad (2)$$

[2] See article by Dr. Albert Ruehli in this Newsletter, page 58.

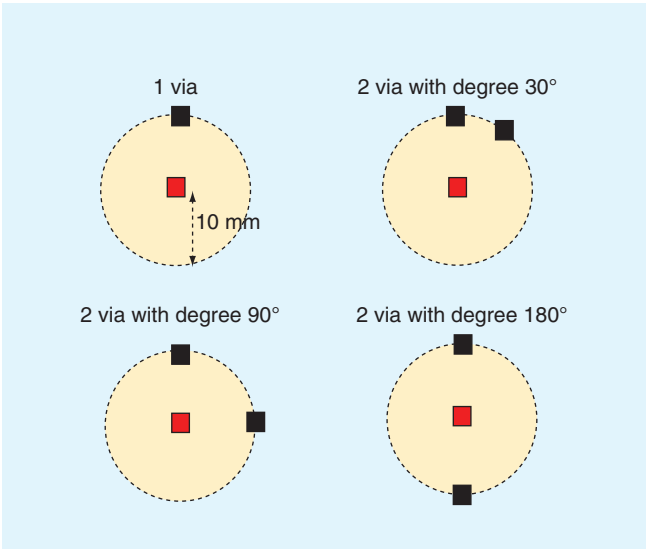

Fig. 5. Shorting via configurations.

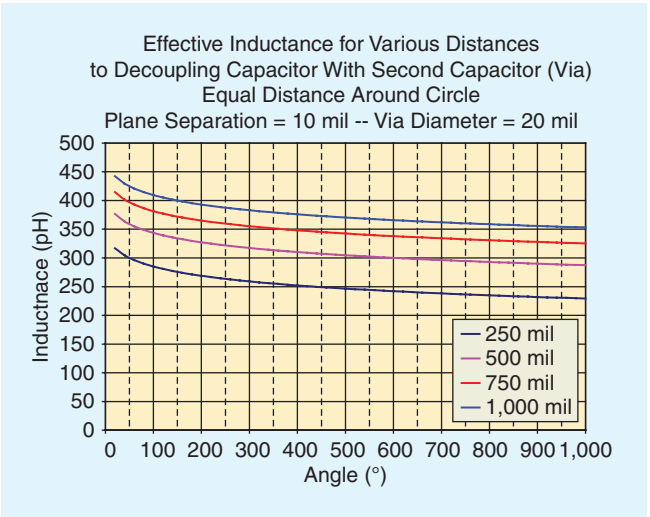

Fig. 8. Effective inductance as second shorting via travels straight (plane separation = 10 mils).

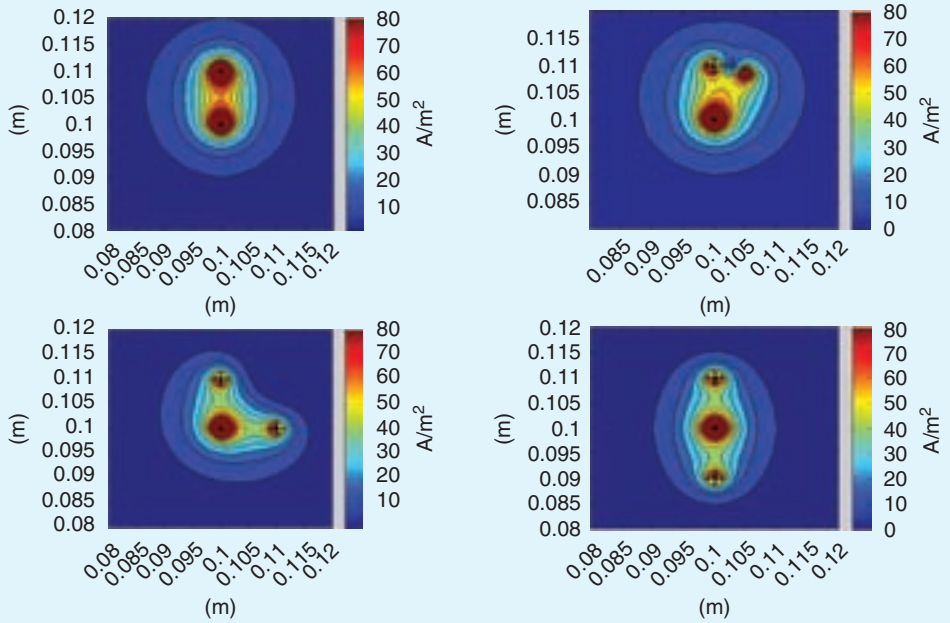

Fig. 6. Current density in planes.

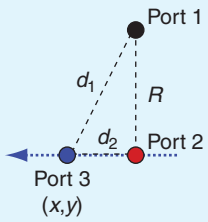

Fig. 7. Shorting via in straight line.

Summary

It is common practice to place multiple decoupling capacitors close together along a side of an IC. While this does provide more capacitance, it does not significantly lower the effective inductance as seen by the power pin of an IC. Placing decoupling capacitors around the IC is more effective in lowering the effective inductance, since the current bunching (current density) is lowered near the decoupling capacitor. However, the current density near the IC power pin remains high, and this results in the effective inductance not being reduced as much as might initially be expected.

References

[1] Jingook Kim, Bruce Archambeault, James Knighten, Jun Fan, "Analysis of Mutual Inductance Effect between Decoupling Capacitors on Planar Power Bus," accepted for publication in the proceedings of the Asia-Pacific EMC Symposium, April 2010, Beijing, China.

[2] A. E. Ruehli, "Inductance Calculations in a Complex Integrated Circuit Environment," IBM Journal of Research and Development, Vol. 16, No. 5, September 1972.

[3] P. A. Brennan, N. Raver, A. E. Ruehli, "Three-dimensional Inductance Computations with Partial Element Equivalent Circuits," IBM Journal of Research and Development, Vol. 23, No. 6. November 1979. **EMC**